REMARKS

STATUS OF THE DRAWINGS

The Office objected to Figure 1 as not being designated by a legend such as –Prior Art-- and required correction in compliance with 37 CFR 1.121(d). A corrected replacement sheet including the legend –Prior Art-- is included herewith.

STATUS OF THE CLAIMS

Claims 1-12 remain in the application. Claims 13-16 have been withdrawn.

The Office rejected Claims 1-12 under 35 U.S.C. 102(e) as being anticipated by *Forcier*.

SUMMARY OF THE INVENTION

The present invention is directed to a microsystem-on-a-chip comprising a bottom wafer of normal thickness and a series of thinned wafers stacked on the bottom wafer, glued and electrically interconnected. The interconnection layer comprises a dielectric material, an interconnect structure, and can include embedded thin-film passives. The use of stacked, thinned silicon chips enable fully 3D, vertical integration.The stacked wafer technology provides a heterogeneously integrated, ultra-miniaturized, higher performing, robust and cost-effective microsystem package.

SUMMARY OF THE ART

Forcier, U.S. 6,919,508, discloses a build-up structure for chip to chip interconnects between chips in the same layer and system-in-package utilizing multi-angle vias for electrical and optical routing or bussing of electronic information. Additional dielectric layers and metal circuitry are formed using the multi-angle vias to form escape routing from tight pitch bond pads on the die to other active and passive components positioned on a substrate.

ARGUMENTS

CLAIMS 1-12, LIMITED TO A THIN UPPER CHIP COMPRISING ONE OR MORE MICROSYSTEM DEVICES CONNECTED BY VIAS IN AN INTERCOONECT LAYER TO ONE OR MORE MICROSYSTEM DEVICES ON A BOTTOM CHIP, ARE NOT ANTICIPATED BY *FORCIER* UNDER 35 U.S.C. § 102(e)

The Office rejected Claims 1-12, asserting that the Applicant's microsystem-on-a-chip is anticipated by *Forcier's* multilayer interconnect structure. To anticipate a claim, the reference must teach each and every element of the claim. *See* MPEP 2131. Applicants submit that *Forcier* does not anticipate Claims 1-12, because *Forcier* does not teach vertical integration of multiple chip layers.

Forcier's interconnect layer 800 comprises electrical vias 820 that connect active or passive components 840 that are embedded in the same layer 830. Therefore, *Forcier* discloses two-dimensional, horizontal integration of these components. Further, *Forcier's* components are discrete devices that are attached to the substrate 850 (e.g., a printed wiring board) with an adhesive. In particular, *Forcier* does not teach a thin upper chip 800, 860 comprising one or more microsystem devices (i.e., active components), as asserted by the Office. *See* Office Action, page 3. There are no active or passive components 840 in *Forcier's* layer 800. Rather, layer 800 is a flex circuit layer comprising vias 820 that connect discrete active components in the same layer 830 or to separate, discrete devices 810 on the surface. *See Forcier*, col. 8 and FIG. 8.

Conversely, Applicant discloses and claim 1 recites a three-dimensional, vertically integrated chip-stacking structure wherein microsystem devices (i.e., active components) 222 fabricated in the bottom chip 220 are connected to microsystem devices 242 fabricated in a thin upper chip 240 by an interconnect structure 238 in a compliant interconnect layer 230. *See* Application pages 9-10, and FIG. 3.

With regards to claim 6, Applicants teach that thin upper chip (i.e., less than 120 microns) is necessary to prevent thermal expansion mismatch between the stacked layers. *See* Application, page 9.

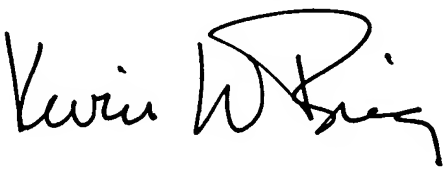
With regards to claim 7, *Forcier's* passive components 840 are discrete passive components that are embedded in a conductive adhesive 830, not in interconnect layer 800. *See Forcier*, col. 8 and FIG. 8. Conversely, Applicant's passive components 238 comprise thin film resistors, capacitors, and inductors that are deposited in interconnect layer 230. *See* Application, page 10, lines 9-12; page 14, lines 11-30; and FIG. 3.

Nowhere does *Forcier* teach a thin upper chip on an interconnect layer, the thin upper chip comprising one or more microsystem devices with associated input/output pads on the top surface of the thin upper chip that are connected to one or more via capture pads in the interconnect layer by conductive vias through the thin upper chip as recited in Applicant's Claim 1. Accordingly, Applicants submit that this rejection is overcome and that Claim 1 is in condition for allowance. Furthermore, Applicant submits that Claims 2-12, that depend from and further define Claim 1, are likewise in condition for allowance. *See* MPEP 2143.03.

CONCLUSION

Applicant urges that the application is now in condition for allowance.

Respectfully submitted,



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CERTIFICATION UNDER 37 CFR 1.8

I hereby certify that this correspondence and documents referred to herein were deposited with the United States Postal Service as first class mail addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on the date shown below.

Date: 2/2/2006 By: Martha Trujillo